RF Silicon MOS Integrated Power Amplifier for Analog Cellular Applications

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ABSTRACT

We report the RF performance of the first Integrated Power Amplifier using silicon MOS Field Effect Transistors, shunt and series capacitors, transmission lines, spiral inductors, ground vias and ESD protection devices. The amplifier provided an output power of 1.5W and 56% efficiency at a supply voltage of 5.8V (850MHz) with 25dB of small signal gain and more than 10dB input return loss.

INTRODUCTION

The main focus of RF technology for the next decade has been shifted from military to personal and consumer products. Cellular telephones, and a whole new generation of personal communications services will command the development of future RF semiconductor technologies. This change of focus brings new trade-offs in cost and performance that a new generation of RF products will have to address. In this paper, we summarize the performance obtained in the development of a low-cost RF Silicon MOS integrated technology suitable for Integrated Power Amplifier (IPA) designs for VHF and RF applications. This technology integrates a silicon RF Power MOS transistor with passive components such as transmission lines, inductors, capacitors, resistors and ESD protection structures. The process is essentially a modification of the discrete LDMOS process flow to incorporate all passive structures necessary for RF integration. Specific process information regarding the fabrication and characterization of the integrated active and passive devices is being submitted as a separate paper to this symposium. [1] This paper focus on the specific IPA circuit requirements, design and measured-vs-simulated performance.

DESIGN AND RESULTS

The RF IPA described in this paper was designed to provide more than 31.5dBm RF output power with a 13dBm input power and a 6V supply voltage for portable wireless analog applications. The overall Power Added Efficiency specifications is greater than 50% at 850MHz. Since output power has to be greater than 1.5W for a 5.8V supply voltage, a 4 cell (about 20 mm of effective gate width) MOS Field-Effect Transistor was chosen for the output stage. This device is capable of more than 2W output power at 5.8V supply voltage. This cell dimension provided enough margin to ensure a minimum output power requirement. With the minimum power added efficiency specification of 50%, the output device is to operate under class AB condition. The quiescent current was chosen to be 140mA. At this bias current, the amplifier can provide a reasonable gain at lower input power while still maintaining high efficiency. The power gain for the 4 cell device at 2W is approximately 11dB. This is about 7.5dB shy of required minimum gain. Hence, a 2-stage power amplifier is needed. To ensure good linearity and drive level (>22dBm) a 1 cell device was chosen for the first stage.

Figure 1 shows the final schematic for the IPA. The initial input and interstage matching were done using measured s-parameter. These matching sections and drain load line were further fine-tuned using the Hewlett Packard Microwave and RF Design Systems (MDS) and Root Large Signal Models for the 2 and 4 cell devices. The load line for the 4 cell can also be done by mounting the 4 cell device in an RF test fixture and tuning the output load line with any commercially available slide screw tuner (e.g. Maury's manual or automated tuner). The load line was chosen such that power, gain and efficiency were optimized. From the MDS simulation results, the best output matching impedance (Gamma L) is about 0.8<166. With this tuned load line, the 4 cell device shows an output power of 31.8dBm, 65% power

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added efficiency and 12dB gain. A two section low pass matching network was used to realize the simulated impedance level. This output matching network was realized using off-chip components because the on-chip Silicon components are too lossy. Figure 2 illustrates the final layout of the integrated power amplifier. Overall die size is 65X65 mils.

The output power and power added efficiency performance of the power amplifier is compared to the simulated performance in Figure 3 and 4, respectively. Figure 5 shows the simulated tuned load lines. The input return loss was better than 10dB and the IPA remained unconditionally stable for all mismatch loads. Measured and simulated small signal data are shown in figure 6. There is a very good correlation between measured and simulated data. Under large signal conditions, the LDMOS IPA achieved 31.5dBm output power with the gain of 19.5dB and power added efficiency of 56.4%.

REFERENCES

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[2] "New Development Trends for Silicon RF Device Technologies", IEEE 1994 Microwave and Millimeter Wave, N. Camilleri, J. Costa, D. Lovelace, D. Ngo

[3] "A Silicon MOS Process for Integrated RF Power Amplifiers", C. Dragon, J. Costa, D. Lamey, D. Ngo, W. Burger, N. Camilleri, submitted to the 1996 IEEE MTT-S.

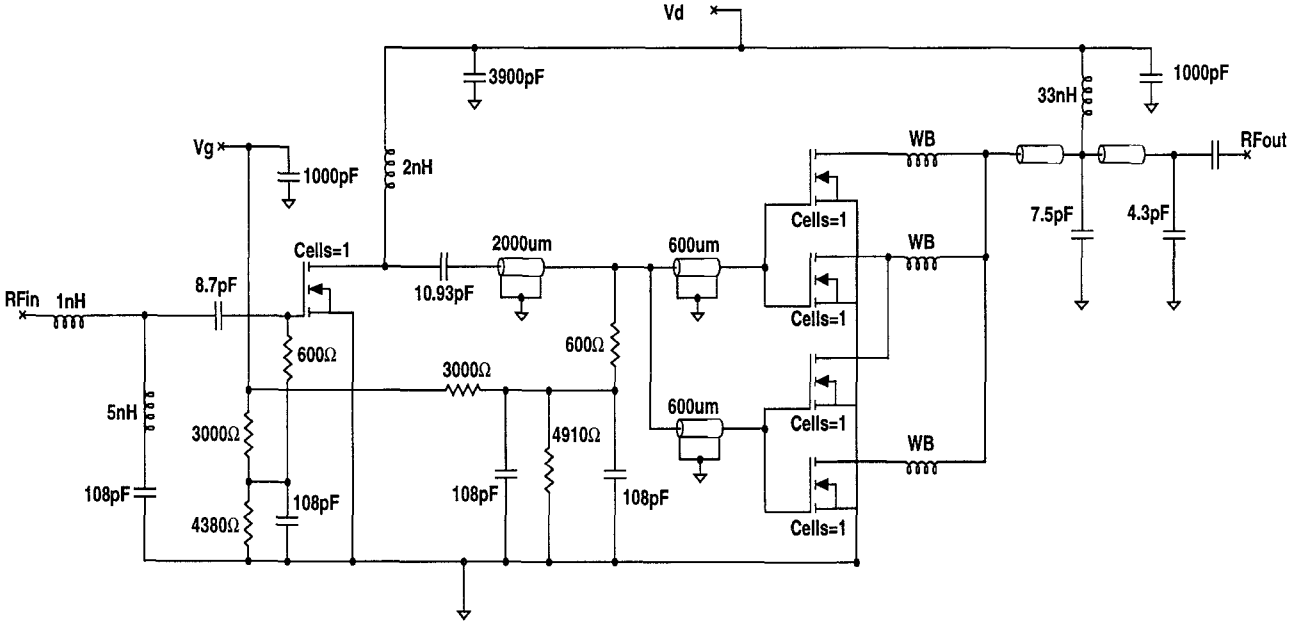

Figure 1. Integrated Power Amplifier schematic.

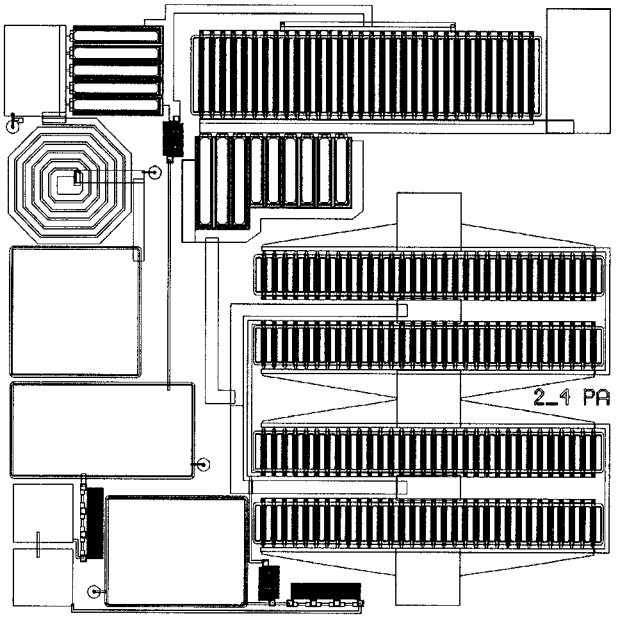

Figure 2. IPA layout (65x65mils).

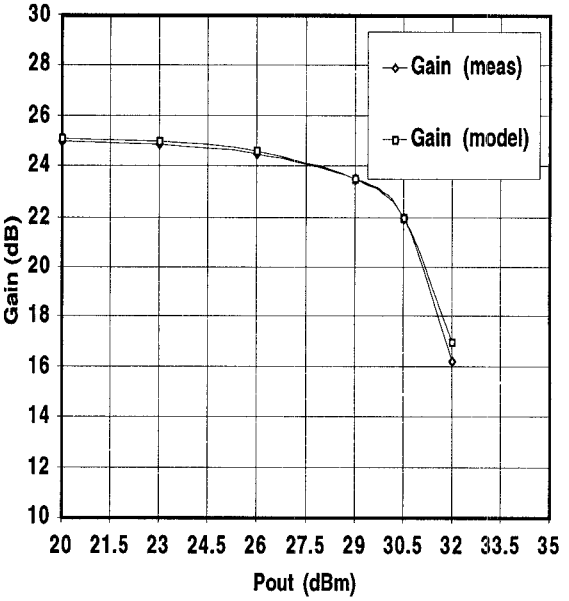

Figure 3. Measured and simulated gain vs output power.

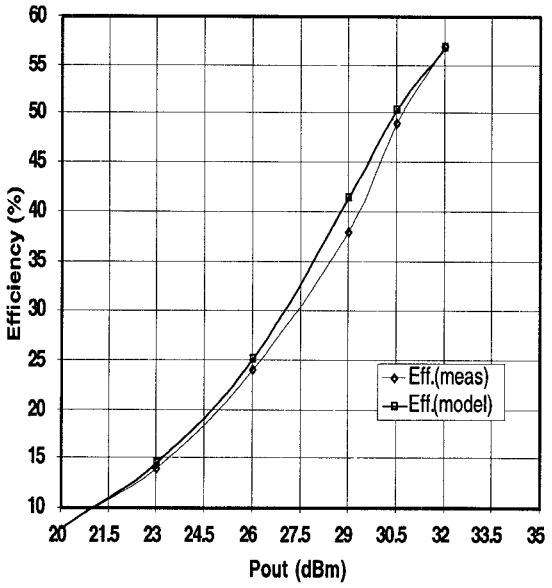

Figure 4. Measured and simulated efficiency vs output power.

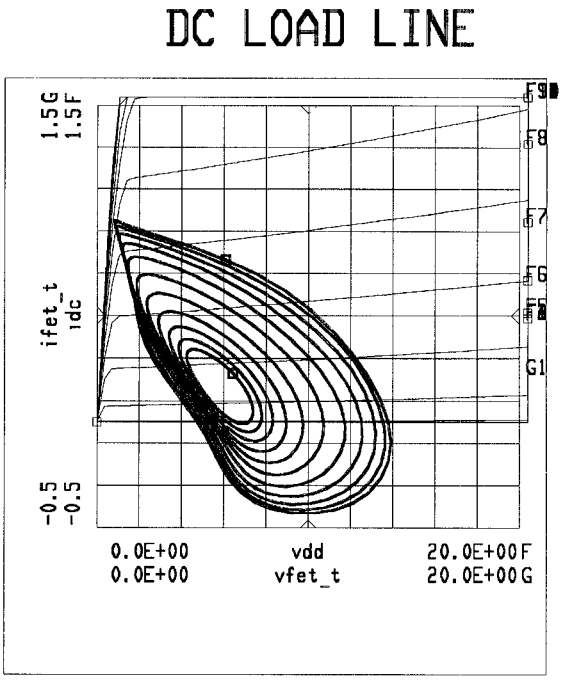

Figure 5. Simulated load lines.

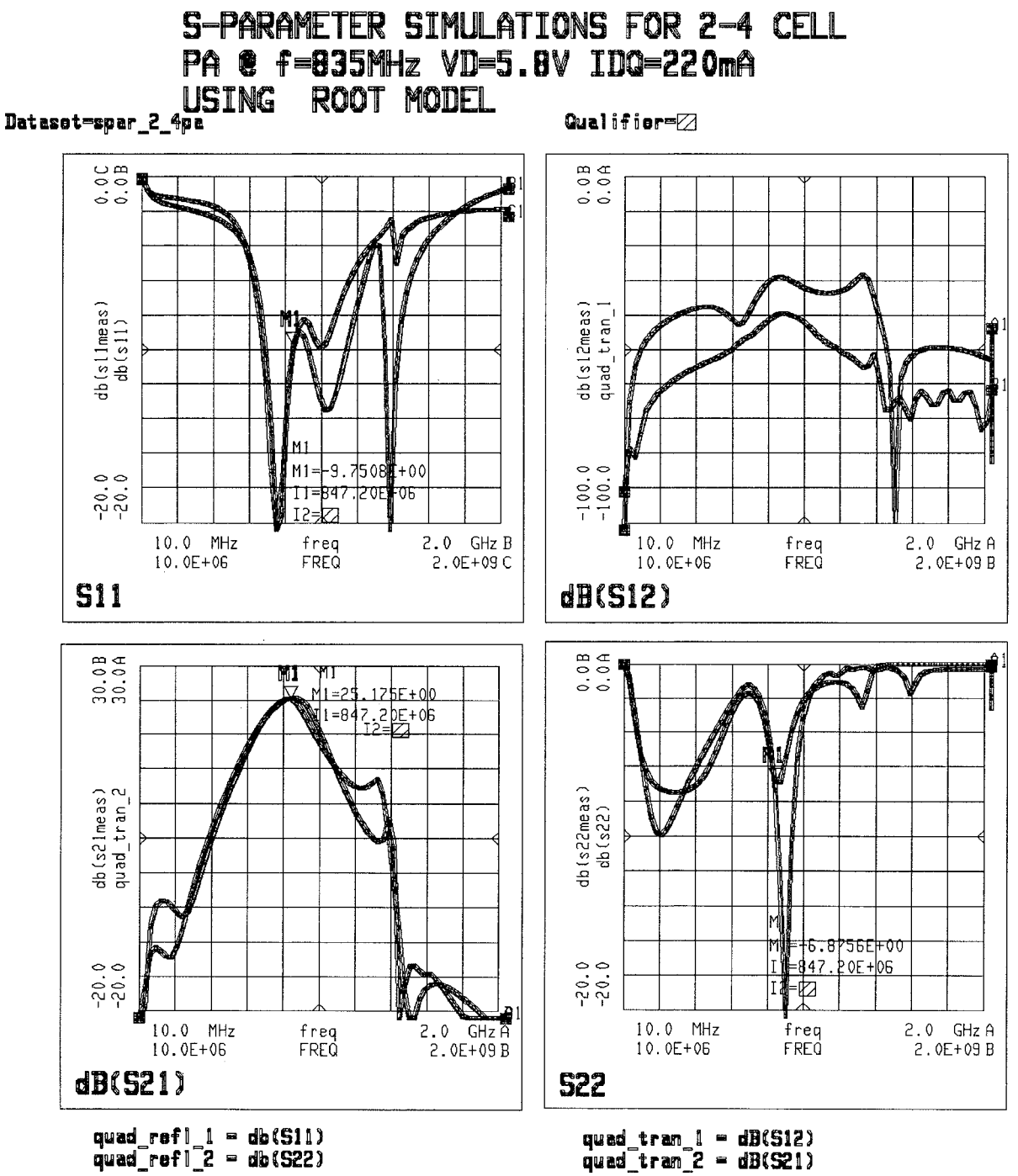

Figure 6. Measured and simulated small signal data.